AMENDMENT TO THE CLAIMS

Please amend the claims as follows:

1. – 19. (Canceled)

20. (Previously presented) A method for forming a semiconductor device, comprising the steps of:

a) forming an insulating film of a carbon-containing silicon oxide film over a substrate;

b) etching the insulating film using a resist pattern as a mask, thereby forming an interconnect groove in the insulating film;

c) performing an etching process, thereby removing a surface film of the resist pattern and forming a silicon oxide layer on an inner face of the interconnect groove ,

d) removing the resist pattern; and

e) filling the interconnect groove with a metal film to form a metal interconnect.

21. (Currently amended) The method of Claim 20, wherein ~~performing and etching process, thereby removing the surface film of the resist pattern and forming~~ the etching process is performed to remove the surface film of the resist pattern and form a silicon oxide layer on the inner face of the interconnect groove at the same time.

22. (Previously presented) The method of Claim 20, wherein the etching process uses an etching gas containing oxygen.

23. (Previously presented) The method of Claim 20, wherein the etching process is formed within plasma ambient at a pressure of 13.3 Pa or more.

24. (Previously presented) The method of Claim 20, wherein the etching process is an anisotropic RIE process.

25. (Currently amended) The method of Claim 20, further comprising [[the steps]] a step of removing the silicon oxide layer, [[existing]] which exists on the inner face of the interconnect groove, after removing the resist pattern and before filling the interconnect groove with the metal film.

26. (Previously presented) The method of Claim 20, wherein the silicon oxide layer has a thickness of 20 nm or less.

27. (Previously presented) The method of Claim 20, wherein the silicon oxide layer has a density of 2.0 g/cm^3 or more.

28. (Previously presented) The method of Claim 20, wherein the metal interconnect is made up of a barrier metal layer and a main interconnect layer.

29. (Currently amended) A method for forming a semiconductor device, comprising the steps of:

a) forming an insulating film of a carbon-containing silicon oxide film over a substrate;

b) etching the insulating film using a resist pattern as a mask, thereby forming an interconnect groove in the insulating film;

c) filling the interconnect groove with a resist film;

d) performing an etching process, thereby removing a first region of the resist film, [[existing]] which exists outside the interconnect groove, and the resist pattern,

e) removing a second region of the resist film, still existing inside the interconnect groove,

f) depositing a metal film on the interconnect groove, and

g) filling the interconnect grove with the metal, [[followed by]] thereby removing metal film outside the interconnect and a surface film of the insulating film.

30. (Currently amended) The method of Claim 29, further comprising a step of forming the surface film on the insulating film when the second region of the resist film, which exists inside the interconnect groove is removed.

31. (Previously presented) The method of Claim 29, wherein the etching process uses an etching gas containing oxygen.

32. (Currently amended) The method of Claim 29, wherein the etching process is ~~carried out~~ formed by a down flow technique in a vacuum of 13.3 Pa or less.

33. (New) The method of Claim 29, wherein the metal film is made up of a barrier metal layer and a main interconnect layer.

34. (Currently amended) The method of Claim 33, wherein the barrier metal layer is a tantalum nitride and the main interconnect layer is copper.

35. (Currently amended) A method for forming a semiconductor device, comprising the steps of:

a) forming an insulating film of a carbon-containing silicon oxide film over a substrate;

b) etching the insulating film using a resist pattern as a mask, thereby forming an interconnect groove in the insulating film;

c) filling the interconnect groove with a resist film;

d) performing a etching process, thereby removing a first region of the resist film ~~existing~~, which exists outside the interconnect groove, and [[a]] the resist pattern,

e) removing a second region of the resist film, ~~existing~~ which exists inside the interconnect groove,

f) forming a silicon oxide layer on an inner face of the interconnect groove,

g) depositing a metal film on the interconnect groove, and

h) filling the interconnect grove with the metal, ~~followed by~~ thereby removing the metal film outside the interconnect and a surface film on the insulating film.

36. (Previously presented) The method of Claim 35, wherein the etching process uses an etching gas containing oxygen.

37. (Currently amended) The method of Claim 35, wherein the etching process is ~~carried out~~ formed by a down flow technique in a vacuum of 13.3 Pa or less.

38. (Currently amended) The method of Claim 35, wherein the ~~surface film comprises a~~ silicon oxide layer on the bottom and side faces of the interconnect groove formed by an anisotropic RIE process in a vacuum of 13.3 Pa or less.

39. (Previously presented) The method of Claim 35, wherein the silicon oxide layer has a thickness of substantially 15 nm or less.

40. (Previously presented) The method of Claim 35, wherein the silicon oxide layer has a density of 2.0 g/cm^3 or more.